Speeding up Digital Systems With Delay Lines

A tapped delay line can produce multiple clock phases very simply. As an example, with a 50MHz input, a DS1100U-20 (5ns per tap) will produce phase shifts of 90°, 180°, and 270° at the Phase 1, Phase 2, and Phase 3 outputs, respectively. Multiple phase clocks can be used to speed up system throughput by allowing multiple actions to occur within a single master clock period, (e.g. set up data and addresses with Phase 1, clock in data on Phase 2, etc.). Sometimes it may even be possible to avoid introducing wait states into the system, a case of using a delay to speed up your system.